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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Docket No.: 303.324US4

Serial No.: 09/691,004

Filed: October 18, 2000

Due Date: February 20, 2003

Examiner: Johannes P. Mondt

Group Art Unit: 2826

**Box AF**

Commissioner for Patents  
Washington, D.C. 20231

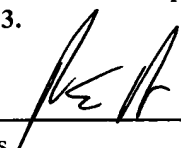
We are transmitting herewith the following attached items (as indicated with an "X"):

☒ A return postcard.

☒ An Amendment and Response under 37 CFR § 1.116 (9 Pages).

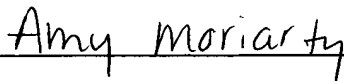
Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
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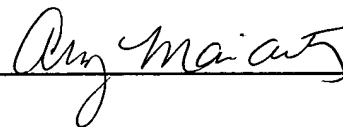
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 31st day of January, 2003.

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P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)